ABSTRACT

A memory system provides one or more control signals for configuring and controlling a memory sub-system during a power failure or system reset. A power delay circuit and a power fail controller cooperate to quickly place the memory system in a retention state in the event a power failure event is detected. The power delay circuit detects either a reset signal or power failure to initiate the memory retention state. The power delay circuit and power fail controller ensure the memory system is initialized prior to entering the retention state.

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